INTEGRATED CIRCUITS

DATA SHEET

TDA8775

Triple 10-bit video Digital-to-Analog Converter (DAC)

Product specification
Supersedes data of 1996 Aug 14

2002 Apr 24

Philips
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FEATURES

- 10-bit resolution
- Sampling rate up to:
  - 50 MHz for normal mode; R_L = 37.5 Ω
  - 35 MHz for LOW power mode; R_L = 150 Ω
- Internal current reference
- Current reference selector for:
  - Normal mode; R_L = 37.5 Ω (typ.)
  - Low-power mode; R_L = 150 Ω (typ.).
- No deglitching circuit required
- $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ control inputs
- 0.66 V output voltage range on red and blue channels
- 1 V output voltage range on green channel (including sync)
- $\overline{\text{BLANK}}$ control input on the 3 channels
- +5 V power supply.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing
- Set-top boxes
- Video games.

GENERAL DESCRIPTION

The TDA8775 consists of three 10-bit video Digital-to-Analog Converters (DACs). They convert the digital input signals into current outputs at a maximum conversion rate of 50 MHz.

The DACs are based on current source architecture with selectable current reference.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	SLT = 1; R_L = 37.5 Ω	–	67	85	mA
		SLT = 0; R_L = 150 Ω	–	16	22	mA
I_{DDD}	digital supply current	SLT = 1; R_L = 37.5 Ω	–	10	16	mA
		SLT = 0; R_L = 150 Ω	–	5	13	mA
INL	DC integral non-linearity	SLT = 1; R_L = 37.5 Ω	–2	–	+2	LSB
DNL	DC differential non-linearity	SLT = 1; R_L = 37.5 Ω	–1	–	+1	LSB
INL	DC integral non-linearity	SLT = 0; R_L = 150 Ω	–2	–	+2	LSB
DNL	DC differential non-linearity	SLT = 0; R_L = 150 Ω	–1	–	+2.3	LSB
$f_{clk(max)}$	maximum clock frequency	SLT = 1; R_L = 37.5 Ω	50	–	–	MHz
		SLT = 0; R_L = 150 Ω	35	–	–	MHz
P_{tot}	total power dissipation	SLT = 1; R_L = 37.5 Ω; f_{clk} = 50 MHz	–	385	555.5	mW
		SLT = 0; R_L = 150 Ω; f_{clk} = 35 MHz	–	105	192.5	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8775G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

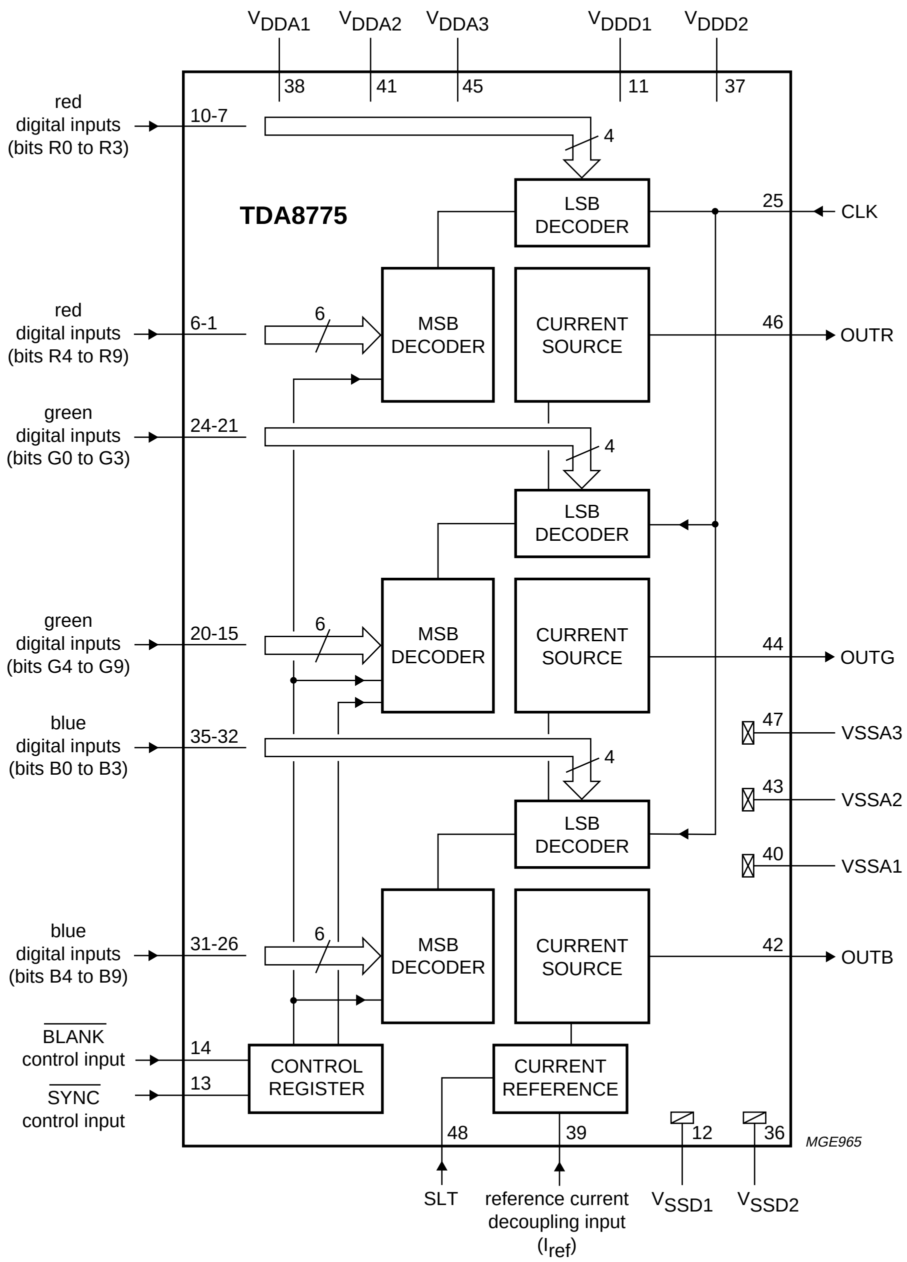


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
R9	1	red digital input data; bit 9 (MSB)
R8	2	red digital input data; bit 8
R7	3	red digital input data; bit 7
R6	4	red digital input data; bit 6
R5	5	red digital input data; bit 5
R4	6	red digital input data; bit 4
R3	7	red digital input data; bit 3
R2	8	red digital input data; bit 2
R1	9	red digital input data; bit 1
R0	10	red digital input data; bit 0 (LSB)
V_{DDD1}	11	digital supply voltage 1
V_{SSD1}	12	digital supply ground 1
$\overline{SYNC}$	13	composite sync control input; for green channel only (active LOW)
$\overline{BLANK}$	14	composite blank control input (active LOW)
G9	15	green digital input data; bit 9 (MSB)
G8	16	green digital input data; bit 8
G7	17	green digital input data; bit 7
G6	18	green digital input data; bit 6
G5	19	green digital input data; bit 5
G4	20	green digital input data; bit 4
G3	21	green digital input data; bit 3
G2	22	green digital input data; bit 2
G1	23	green digital input data; bit 1
G0	24	green digital input data; bit 0 (LSB)
CLK	25	clock input
B9	26	blue digital input data; bit 9 (MSB)
B8	27	blue digital input data; bit 8
B7	28	blue digital input data; bit 7
B6	29	blue digital input data; bit 6
B5	30	blue digital input data; bit 5
B4	31	blue digital input data; bit 4
B3	32	blue digital input data; bit 3
B2	33	blue digital input data; bit 2
B1	34	blue digital input data; bit 1
B0	35	blue digital input data; bit 0 (LSB)
V_{SSD2}	36	digital supply ground 2
V_{DDD2}	37	digital supply voltage 2
V_{DDA1}	38	analog supply voltage 1
I_{ref}	39	decoupling pin for reference current
V_{SSA1}	40	analog supply ground 1

SYMBOL	PIN	DESCRIPTION
V_{DDA2}	41	analog supply voltage 2
OUTB	42	blue analog output
V_{SSA2}	43	analog supply ground 2
OUTG	44	green analog output
V_{DDA3}	45	analog supply voltage 3
OUTR	46	red analog output
V_{SSA3}	47	analog supply ground 3
SLT	48	mode selection; normal mode, R_L = 37.5 Ω (active HIGH); low power mode, R_L = 150 Ω (active LOW)

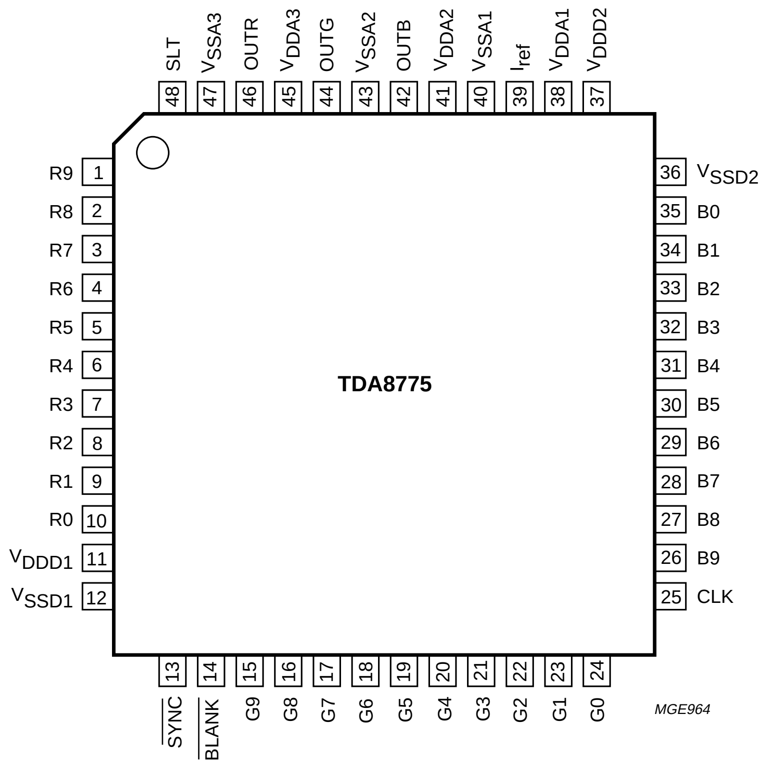


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	–0.5	+6.5	V
V_{DDD}	digital supply voltage	–0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	–1.0	+1.0	V
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
T_j	junction temperature	–	125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE (TYP.)	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	72	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

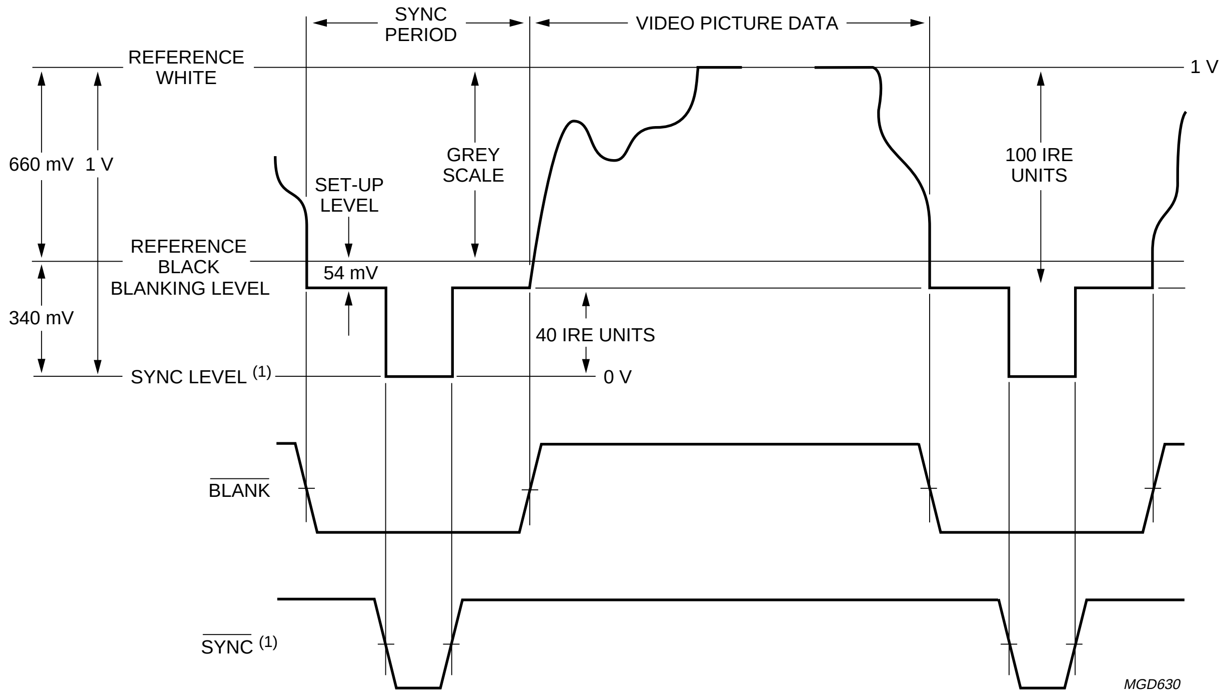
TDA8775 operating at 50 MHz; SLT = 1 and R_L = 37.5 Ω. V_{DDA} = V_{DDD} = 4.5 to 5.5 V; V_{SSA} and V_{SSD} shorted together; V_{DDA} – V_{DDD} = –0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical values measured at V_{DDA} = V_{DDD} = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	SLT = 1; R_L = 37.5 Ω	–	67	85	mA
		SLT = 0; R_L = 150 Ω	–	16	22	mA
I_{DDD}	digital supply current	SLT = 1; R_L = 37.5 Ω	–	10	16	mA
		SLT = 0; R_L = 150 Ω	–	5	13	mA
Inputs						
CLOCK INPUT (PIN 25)						
V_{IL}	LOW level input voltage		V_{SSD} – 0.5	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD} + 0.5	V
$\overline{\text{BLANK}}$ AND $\overline{\text{SYNC}}$ INPUTS (PINS 13 AND 14; ACTIVE LOW)						
V_{IL}	LOW level input voltage		V_{SSD} – 0.5	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD} + 0.5	V
R, G AND B DIGITAL INPUTS (PINS 1 TO 10, 15 TO 24 AND 26 TO 35)						
V_{IL}	LOW level input voltage		V_{SSD} – 0.5	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD} + 0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing; see Fig.4						
$f_{clk(max)}$	maximum clock frequency	SLT = 1; R_L = 37.5 Ω	50	–	–	MHz
		SLT = 0; R_L = 150 Ω	35	–	–	MHz
t_{CPH}	clock pulse width HIGH		6	–	–	ns
t_{CPL}	clock pulse width LOW		6	–	–	ns
t_r	clock rise time		–	–	4	ns
t_f	clock fall time		–	–	4	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns
Outputs						
OUTB, OUTR AND OUTG ANALOG OUTPUTS (PINS 42, 46 AND 44, REFERENCED TO V_{SSA}) FOR 37.5 Ω LOAD						
V_{OUTmax}	maximum output voltage	$\overline{BLANK}$ and $\overline{SYNC}$ active				
		R and B channels	–	0.714	–	V
		G channel	–	1.0	–	V
THD	total harmonic distortion	f_i = 4.43 MHz; SLT = 1; f_{clk} = 50 MHz; R_L = 37.5 Ω (filter; see Fig.8)	–	–60	–	dB
Z_L	output load impedance	SLT = 1	–	37.5	–	Ω
		SLT = 0	–	150	–	Ω
Transfer function						
INL	DC integral non-linearity	SLT = 1; R_L = 37.5 Ω	–2	–	+2	LSB
DNL	DC differential non-linearity	SLT = 1; R_L = 37.5 Ω	–1	–	+1	LSB
INL	DC integral non-linearity	SLT = 0; R_L = 150 Ω	–2	–	+2	LSB
DNL	DC differential non-linearity	SLT = 0; R_L = 150 Ω	–1	–	+2.3	LSB
α_{ct}	crosstalk DAC to DAC	SLT = 1; R_L = 37.5 Ω; T_{amb} = 25 °C	–	–73	–	dB
	DAC to DAC matching	SLT = 1; R_L = 37.5 Ω; $\overline{SYNC}$ = 0; $\overline{BLANK}$ = 1	–5.5	1.5	+5.5	%
Switching characteristics; see Fig.5						
t_d	input to 50% output delay time	full-scale change; SLT = 1; R_L = 50 Ω	–	3.5	–	ns
t_{s1}	settling time	10 to 90% full-scale change; SLT = 1; R_L = 50 Ω	–	1.2	–	ns
t_{s2}	settling time	to ±1 LSB; SLT = 1; R_L = 50 Ω	–	3	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change	SLT = 1; R_L = 50 Ω	–	300	–	LSB.ns

Table 1 Input coding and DAC output currents (typical values)

BINARY INPUT				DAC OUTPUT CURRENT (mA) SLT = 1; R_L = 37.5 Ω		DAC OUTPUT CURRENT (mA) SLT = 0; R_L = 150 Ω	
$\overline{SYNC}$	$\overline{BLANK}$	DATA	CODE	R, B Channels	G Channel	R, B Channels	G Channel
0	0	XXH	–	0	0	0	0
1	0	XXH	–	0	7.62	0	1.90
0	1	00H – 3FFH	0 – 1023	1.44 – 19.05	1.44 – 19.05	0.36 – 4.76	0.36 – 4.76
1	1	00H – 3FFH	0 – 1023	1.44 – 19.05	9.05 – 26.67	0.36 – 4.76	2.26 – 6.67



(1) Sync only on green channel.

Fig.3 Video signal diagram.

TIMING

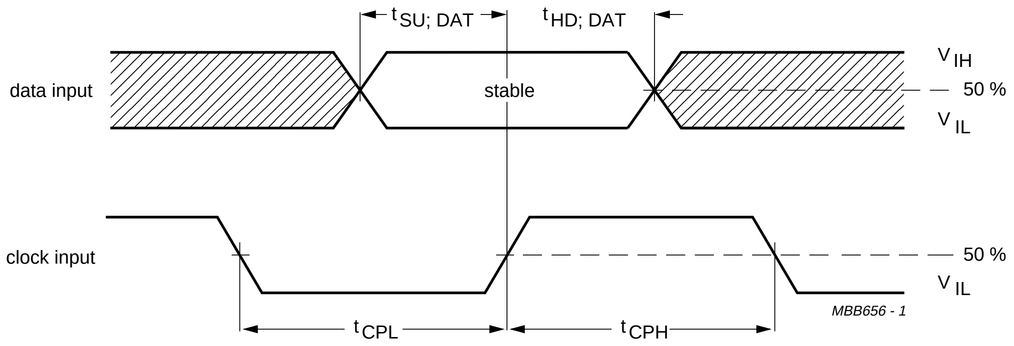
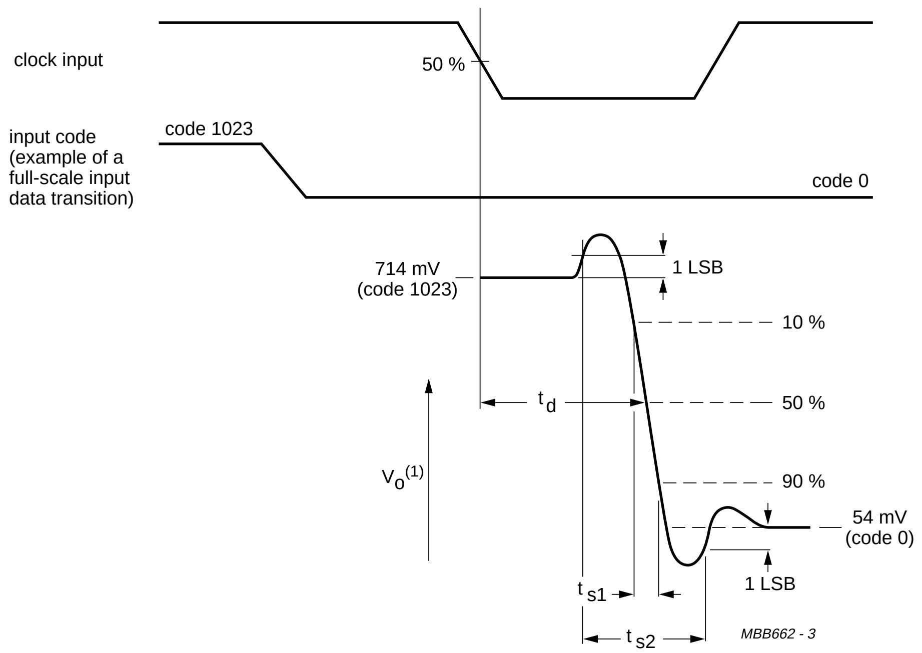


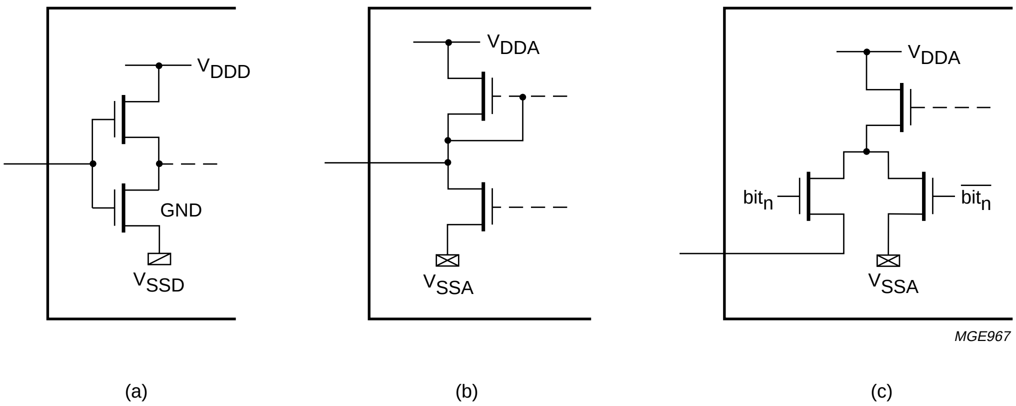
Fig.4 Input timing.



(1) Output level conditions, $\overline{SYNC}$ = 0; $\overline{BLANK}$ = 1.

Fig.5 Switching timing.

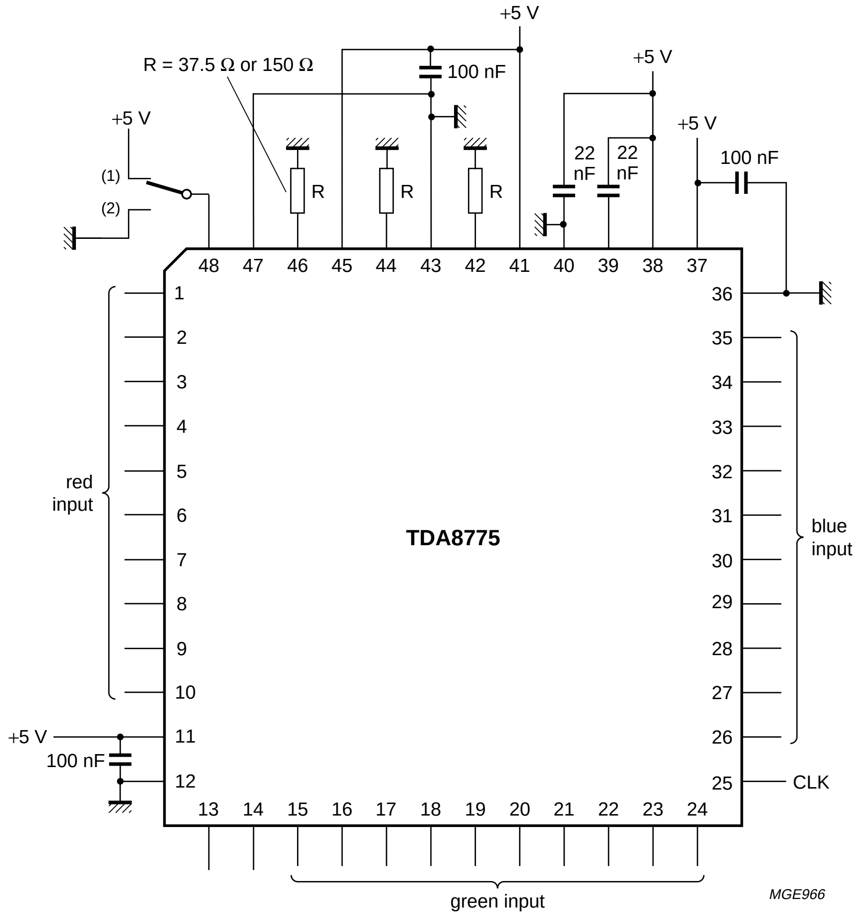
INTERNAL PIN CIRCUITRY



(a) Digital inputs; pins 1 to 10, 13 to 25 and 26 to 35.
(b) I_{ref}; pin 39.
(c) OUTR, OUTG and OUTB; pins 46, 44 and 42.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.

Supplies are not connected internally.

All ground pins must be connected. One ground plane is preferred although it depends on the application.

(1) R = 37.5 Ω; SLT = 1.

(2) R = 150 Ω; SLT = 0.

Fig.7 Application diagram.

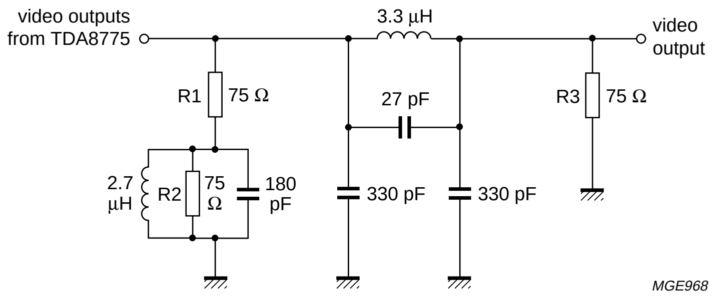
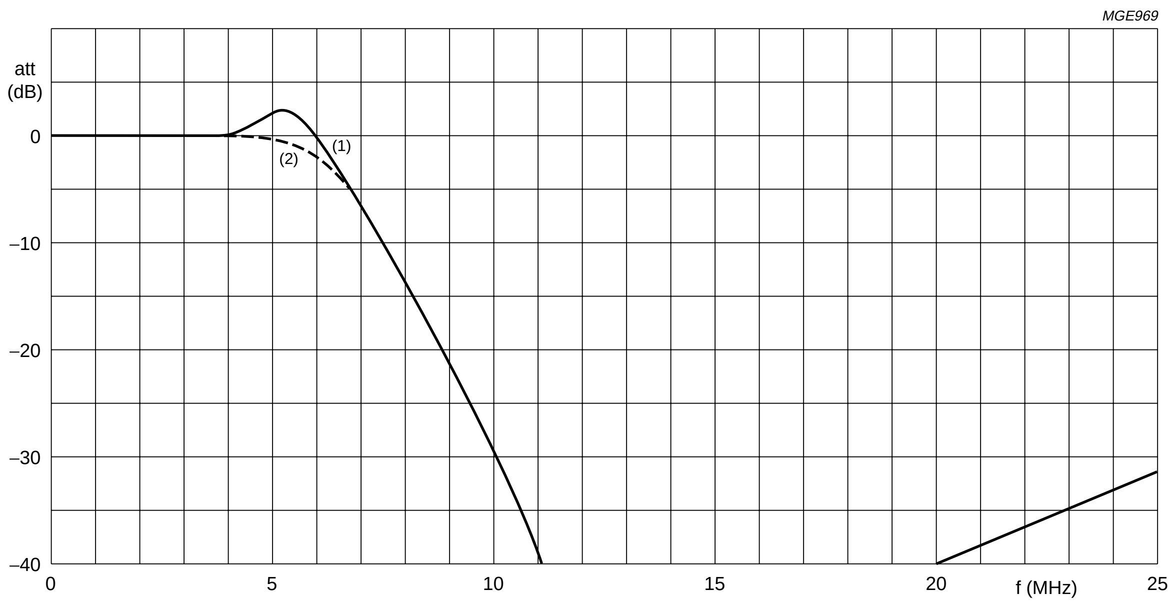


Fig.8 Example of reconstruction filter for 1 V output swing.



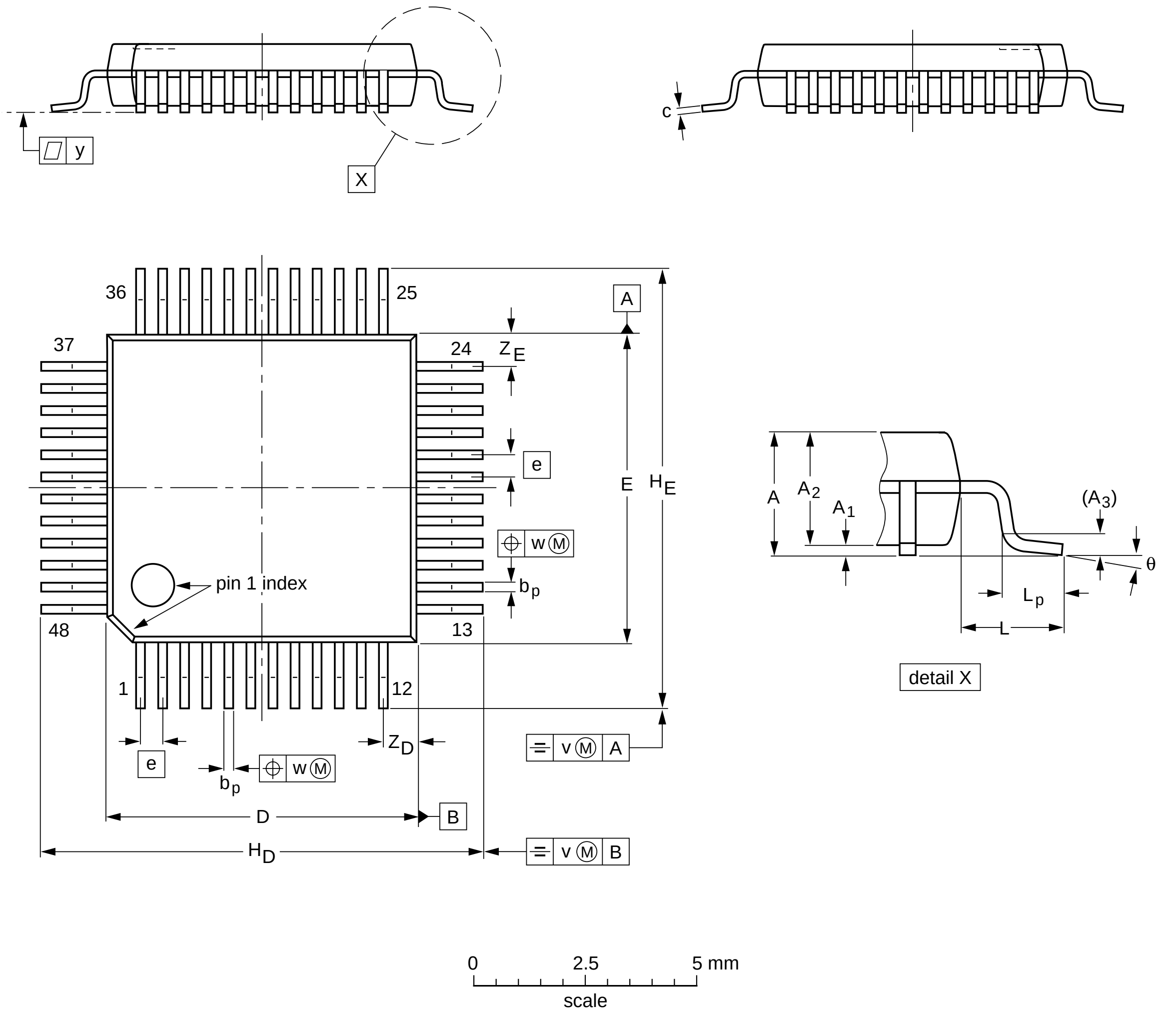
(1) R2 = 75 Ω.

(2) R2 = 0 Ω.

Fig.9 Frequency response for filter shown in Fig.8.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**

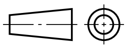


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[(1)]	PRODUCT STATUS[(2)]	DEFINITIONS
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Notes

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